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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,802	01/15/2004	Dae-Woong Kang	8750-042	6500

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/758,802	KANG ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29-36* is/are allowed.

6)☒ Claim(s) *22-28 and 37* is/are rejected.

7)☒ Claim(s) *38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on December 8, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22-28 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 6,642,105 B2).

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 22, Kim et al. shows (fig. 32) a semiconductor device, comprising: a semiconductor substrate having a low voltage region (b) and a high voltage region (a); a first isolation layer (309 right) formed in the low voltage region and defining a first active

region (1b); a second isolation layer (309 left) formed in the high voltage region and defining a second active region (1a); a low voltage gate insulation (305b) layer formed on the first active region; and a high voltage gate insulation layer (305a) formed on the second active region and having a greater thickness than the low voltage gate insulation layer. A step region between the high voltage gate insulation layer and the second isolation layer has no recessed region, wherein a bottom portion of the step region is spaced apart from a vertical axis passing through an edge corner of the second active region toward the second active region toward the second isolation layer adjacent to the vertical axis because the bottom of the step region is not formed directly on the vertical axis.

In re claim 23, Kim shows (fig. 32) a low voltage gate electrode (FG) formed on the low voltage gate insulation layer and disposed to cross over the first active region', and a high voltage gate electrode (313a) formed on the high voltage gate insulation layer and disposed to cross over the second active region.

In re claims 24 and 25, Kim discloses (col. 2, lines 44-50) that the low voltage region is a memory cell region. Kim shows in (fig. 31b) that the low voltage gate insulation layer is a tunnel oxide layer.

In re claim 26, Kim shows (fig. 32) that a control gate electrode (CG) is formed over the low voltage gate insulation layer (305b), the control gate electrode crossing over the first active region; a floating gate (FG) is interposed between the control gate electrode and the low voltage gate insulation layer; a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode (313a) crossing over the

second active region; a dummy gate electrode (317a) stacked on the main gate electrode; and an inter-gate dielectric layer (315a) interposed between the floating gate and the control gate.

In re claim 27, Kim shows (fig. 32) that a thermal oxide (311) layer is interposed between the first isolation layer (309 right) and the semiconductor substrate, and between the second isolation layer (309 left) and the semiconductor substrate.

In re claim 28, Kim shows (fig. 32) that an edge region of the first isolation layer (307) is lower than a top surface of the low voltage gate insulation layer because the low voltage gate insulation layer (305b) is formed on top of the edge of the isolation trench.

In re claim 37, Kim shows (fig. 32) that substantially the entire step region is spaced apart from the vertical axis passing through the edge corner of the second active region since the step region is not formed exactly over the vertical axis.

Allowable Subject Matter

Claim 38 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 29-36 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art references, alone or in combination, do not show a first active region having a protruded edge portion that extends above the top surface. The closest prior art reference, Chen

et al. (US Pub. 2005/0199914 A1) shows (fig. 2H) a protruded edge portion (40), but does not show that the protruded edge portion extends above the top surface of the active region. Chen cannot be combined with Kim because Chen discloses a memory cell device having a floating gate formed in a trench in which the protruding edge injects electrons into the floating gate, whereas Kim only shows a trench isolation structure for separating active regions. The two devices are different and thus one of ordinary skill in the art could not look to Chen to find motivation for modifying or improving Kim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments with respect to claims 22-28 have been considered but are not persuasive. The applicant primarily asserts that Kim et al. does not disclose all of the elements of the claims, specifically the limitation of the bottom portion of the step region spaced apart from a vertical axis passing through an edge corner of the second active region. The examiner believes that Kim et al. shows all of the elements of the claims including the limitation in question. As stated in the rejection above, Kim shows in fig. 32 that the step portion (the portion of isolation 309 above the substrate) has sloped side surfaces that are not formed exactly on the vertical axis imagined at the edge corner of the active region. It looks as if the step portion is larger than the trench

that it is in and therefore the step portion would overlap and extend onto the active surface (or top of the substrate). If this is the case, then the bottom portion of the step region would still be spaced apart from the vertical axis. As long as the step region is not formed directly on the vertical axis, then this limitation is met by Kim. Therefore Kim shows all of the elements of the clams, and this action is made final.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakamura et al. (US 5,783,491) shows (figs. 5D and 5E) a substrate having protruded edge portions, but such portions are taught to reduce the quality and reliability of the device. Chen et al. (US Pub. 2005/0199914 A1) shows (fig. 2H) a substrate having a protruded edge portion (40), but does not show that the protruded edge portion extends above the top surface of the active region. Chen cannot be combined with Kim because Chen discloses a memory cell device having a floating gate formed in a trench in which the protruding edge injects electrons into the floating gate, whereas Kim only shows a trench isolation structure for separating active regions. The two devices are different and thus one of ordinary skill in the art could not look to Chen to find motivation for modifying or improving Kim.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW
February 21, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER